Abstract

Deploying Deep Neural Networks (DNNs) on edge computing devices can be difficult due to resource constraints when faced with the high compute and memory demands of DNNs. Field Programmable Gate Arrays (FPGAs) provide a promising solution to design and create optimised hardware accelerators that require low power consumption and provide high throughput. Existing methods for designing FPGA-based DNN accelerators face the challenge of high development costs in terms of development time. These development costs include repeated FPGA synthesis, translating simulation models to HDL and accelerator integration with target DNN framework.

In this poster, we present SECDA, a new hardware/software co-design methodology that reduces the development time required to design, test and integrate FPGA-based DNN accelerators. SECDA uses cost-effective SystemC simulation alongside hardware execution to reduce the time needed to evaluate each design iteration, thus reducing the development time necessary to arrive at the final design.